DUAL ACCESS SERIAL PERIPHERAL INTERFACE

ABSTRACT OF THE DISCLOSURE

A dual access peripheral interface uses a shared data bus (16) for communication with dual master units (30,32) coupled to a common peripheral device (34). Each master control unit provides a shared subset of control bits to a logic configuration block (48), which combines the control bits in a logic operation to present to the slave peripheral unit (34). The logic configuration block (48) is configured by configuration bits accessible by only one of the master units (30). In this way, both of the master units can access the peripheral at the same time with the logic of the logic configuration block determining the ultimate control of the peripheral.